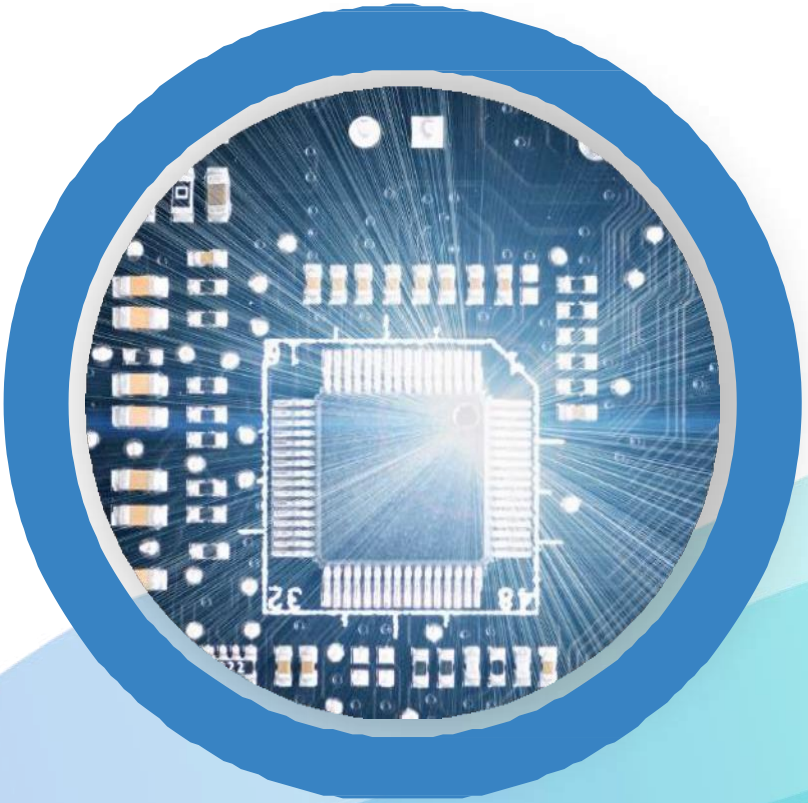
NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY NOIDA

INTERNSHIP/TRAINING PROGRAM ON VLSI DESIGN FLOW (RTL TO GDS-II) (ONLINE MODE)

INFORMATION BROCHURE



NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY, NOIDA

Name of Group: Centre of Excellence in Chip Design at NIELIT NOIDAin association with SoCTeamup Semiconductors Pvt Ltd as industry partner

Name of Course: Internship/Training Program on VLSI Design flow (RTL to GDS-II) **(Online Mode)**

Objective: The Internship/Training in Program on VLSI Design flow (RTL to GDS-II) (Online Mode) aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing. Participants will gain hands-on experience with open source **EDA toolsuite**, explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

Duration: 30 Days/ 06 Weeks (90 Hours) (3 hrs/day) (1hr Theory, 1hr Practical, I hr additional Lab access)

Mode of Delivery: Online mode

Eligibility: B.Tech/M.Tech/B.Sc/M.Sc / or (Diploma in relevant field with min Two Year Industry Experience)
Note: Research Scholars, Faculty members and **Industry professionals** can also enroll
Prerequisites: -

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL
3. Familiarity with a Unix/Linux environment and command-line interface

Course Fees: Rs. 2700/- (incl. GST)

Course Date: 7-October-2024 (Tentative)

Registration Process: Candidates have to apply in prescribed application form through online registration portal https://regn.nielitvte.edu.in/ or through Android App "**NIELIT Kaushal Setu**". The duly filled form along with the course fees has to be submitted in online mode through the above link. The Fees deposited is Non-Refundable.

Topics to be Covered

- **Overview of VLSI Design Flow**
- **Hardware Modeling: Introduction to Verilog-I**
- **RTL Synthesis**
- **Static Timing Analysis**
- **Basic Concepts for Physical Design**
- **Floorplanning,clock tree synthesis,routing**

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Week No	Lecture No	Lecture Title	Concepts Covered
Week 1	Module 1	Basic Concepts of Digital Electronics	This lecture gives Brief Introduction to Basic logic circuits: Logic gates (AND, OR, NOT, NAND, NOR, Ex-OR, ExNOR and their truth tables,), Universal Gates,Combinational Logic. CMOS,CMOS as Inverter ,Nand gate.
	Module 2	Sequential Circuits	This lecture describes Flip flop and Timing circuit :Flip flops D,T,SR Flip flop. Registers & counters:Synchronous/Asynchronous counter operation,Up/down synchronous counter, application of counter.
	Tutorial 1	Introduction to LINUX	This tutorial describes creating a LINUXenvironment using Windows Subsystem for Linux (WSL) in a Windows operating system Then, it describes a few essential UNIX commands.
Week 2	Module 3.	Overview of VLSI Design Flow	This lecture describes the role of logic synthesis in VLSI design flow. It describes various terminologies associated with netlists generated by . Further, it briefly describes various tasks involved in RTL synthesis, logic optimization, and technology mapping.
	Module 4	Overview of VLSI Design Flow	This lecture describes the role of physical design in VLSI design flow. It briefly explains various design tasks involved in physical design, such as chip planning, placement, clock tree synthesis (CTS), routing.
	Module 5	Hardware Modelling using Verilog	This lecture describes HDL for various combinational circuits
	Tutorial 2	Introduction to iverilog	This tutorial introduces simulation using iverilog
Week 3	Module 6	Hardware Modeling: using Verilog	This lecture highlights the distinct features of hardware description languages (HDL) compared to other high-level programming languages. Further, it introduces the Verilog language, identifiers, four-

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			valued data, Verilog nets, variables, vectors, and arrays.
	Module 7	Hardware Modeling: Introduction to Verilog-II	This lecture describes various Verilog language constructs, especially modules, ports, instantiation, and parameterized modules. It also explains operators, expressions, conditional blocks, loop controls, initial blocks, always blocks, functions, and tasks. It also describes the differences between continuous, blocking, and non-blocking assignments.
Week 4	Module 8	RTL Synthesis- Part I	This lecture explains the role of RTL synthesis in VLSI design flow and its various tasks, such as lexical analysis, parsing, elaboration, translation, and optimization.Additionally, it explains the synthesis of assign statements, conditional blocks, always block, inference of flip-flops/latches, and synthesis of blocking and non-blocking assignments.
	Module 9	Logic Optimization: Part I	This lecture highlights the role of logic optimization in VLSI design flow. It discusses two-level logic minimization for incompletely specified Boolean functions. Then, it briefly describes heuristic two-level logic minimization.
	Tutorial 3	Synthesis using Yosys-I (Tentative)	
	Module 10	Logic Optimization: Part II	This lecture discusses multi-level logic minimization for a Boolean logic network using transformations such as simplify, eliminate, substitute, and extract. It also highlights the opportunities and challenges of optimizing using an algebraic model compared to a Boolean model.
	Tutorial 4	Synthesis using Yosys-II (Tentative)	
Week 5	Module 11	Static Timing Analysis	This lecture explains the basic concepts and motivation for static timing analysis (STA) in VLSI design flow. Further, it explains how an STA tool models these constraints using arrival time and required time.
	Module 12	Static Timing Analysis	This lecture explains the mechanics of static timing analysis (STA), which will help designers analyze the timing reports generated by the STA tools and take corrective measures if needed. Specifically, it describes various kinds of paths in a circuit from the perspective of STA, delay

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			calculation, arrival/required time calculation, and slack computation.
	Module 13	Static Timing Analysis-	This lecture explains two types of slew propagation in static timing analysis (STA): graph-based analysis (GBA) and path-based analysis (PBA). multi-mode multi-corner (MMMC) analysis, and on-chip variations (OCV) derating factors.
	Tutorial 5	Static Timing Analysis using OpenSTA-I (Tentative)	
Week 6	Module 14	Constraints I	This lecture discusses the role of constraints, typically written in synopsys design constraints (SDC) format, in VLSI design flow. Further, it explains how these constraints can be specified for clock sources and their attributes, such as latency, uncertainty, and transition.
	Module 15	Technology Mapping	This lecture explains the role of technology mapping in VLSI design flow. It illustrates various trade-offs involved in technology mapping, its opportunities, and challenges.
	Module 16	Basic Concepts for Physical Design	This lecture describes some concepts that are essential in appreciating physical design tasks. It also explains the antenna effect and information contained in library exchange format (LEF) files.
	Module 17	Floorplanning,clock tree synthesis,routing	This lecture describes various tasks involved in clock tree synthesis (CTS), including its target of minimizing the clock skew. It discusses various global clock distribution networks and local clock distribution networks.
	Tutorial 6	Physical Design using OpenRoad-I (Tentative)	

* There will be 2 Hours Session per day in **online mode**.

Mode of Payment: Fees can be paid either by debit/credit card or in any online mode.
For any queries and more details please contact on **8218724641/9711177638**

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Course Venue: Online

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahampurtra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

Registration Link:

https://regn.nielitvte.edu.in

or

Through Android App "**NIELIT Kaushal Setu**"

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